semiconductor device.

B1 Cont'd

13. (Amended) An array as set forth in claim 11, wherein said semiconductor material comprises oriented single crystal grain, monocrystalline semiconductor material, and each of said nodes comprises a diode.

B2

16. (Amended) An array as set forth in claim 15, wherein a first insulating layer is disposed over an upper surface of said upper layer and a second insulating layer is formed over said upper surface of said lower layer, and wherein a second gate electrode is deposited upon said first insulating layer above each field effect transistor.

17. (Amended) An array as set forth in claim 13, wherein said oriented single crystal grain semiconductor material is oriented in the <100> orientation.

18. (Amended) An array as set forth in claim 11, wherein said electrically conducting material comprises at least one of W, Ti, and Ta.

Please add the following new claims:

B3 Cont'

-- 26. A microelectronic element array comprising:

a semiconductor substrate;

a first dielectric layer formed on said substrate;

a plurality of electrically isolated conductive regions disposed within said first dielectric layer, each conductive region comprising a conductive via;

a second dielectric layer having a lower surface which is bonded to an upper surface of said first dielectric layer; and

a plurality of semiconductor nodes formed in said second dielectric layer, each node being in electrical contact with said via.

27. The array according to claim 26, wherein said plurality of semiconductor nodes comprises a plurality of monocrystalline semiconductor diodes.

28. The array according to claim 26, wherein each conductive region extends from said substrate to said upper surface of said first dielectric layer.

29. The array according to claim 26, wherein each conductive region further comprises a word line, said via being formed on said word line.

30. The array according to claim 27, further comprising:

a plurality of magnetic tunnel junction (MTJ) elements, each MTJ element in electrical contact with a diode in said plurality of monocrystalline semiconductor diodes.

B3 Cncl

31. The array according to claim 30, wherein each said MTJ element and each said diode combine to form a memory element.

32. The array according to claim 26, further comprising:

a plurality of field effect transistors, each node in said plurality of semiconductor nodes forming a part of each field effect transistor,

wherein each field effect transistor forms a memory element.

33. The array according to claim 26, wherein said via includes therein at least one of W, Ti, and Ta.

34. The array according to claim 26, wherein each said conductive region further comprises a metal layer in electrical contact with said via, said metal layer being formed of a different material than said via.

35. The array according to claim 29, wherein said via includes therein a refractory metal and said word line comprises one of copper and aluminum. - -